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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,624	10/28/2003	Ulf Tohsche	INFN/0033	6423

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/695,624	TOHSCHE, ULF	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,8-11 and 15-20* is/are allowed.

6)☒ Claim(s) *1-4 and 12-14* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 2/22/05.

2. The objections to the drawings in the last office action have been overcome based on applicant's amendment.

Claim Objections

3. Claims 6, 7 and 12-14are objected to because of the following informalities:

Claim 6, line 2, "having the reset" should be changed to --having an inverted version of the reset-- to avoid the claim being misdescriptive since the NAND and NOR gates of the second feedback look does not receive the same reset signal (see Figure 4).

Claim 7 is objected to because it includes the informality of claim 6.

Claim 12, line 6, "respectively," should be changed to --respectively;--.

Claim 12, line 7, newly added recitation "wherein the first feedback loop comprises;" should be deleted to avoid the claim being indefinite since it is not clear "comprises what".

Claims 13-14 are objected to because they include the informalities of claim 12.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakagami (JP 62-40816).

With respect to claim 12, Figure 19 of the Sakagami reference discloses a flip-flop, which includes: a clock signal (ø), non-inverted (DO) and inverted (DO/) output nodes; data signal (DI); a first holding element (first feedback loop 18_1-18_2 comprises inverters controlled by the clock signal) having first node (N3) and second node (N4); and a second holding element (second feedback loop 18_3-18_4 comprises inverters controlled by the clock signals) having a third node (N6) and a fourth node (N5). Note that when clock ø goes to Hi (first edge of the clock), then non-inverted and inverted logic levels of the data signal (DI) are transferred to the first and second nodes, respectively; and when clock ø goes to Lo (second edge of the clock), the non-inverted logic level at the first node is transferred to the non-inverted output node (DO) via the fourth node (N5; note that the propagation delay for this path is two inverters and one transmission gate delay), and the inverted logic level at the second node is transferred to the inverted output node (DO/) via the third node (N6; note that the propagation delay for this path is two inverters and one transmission gate delay). Note that the propagation gate delay from the first node to the non-inverted output equals the propagation delay from the second node to the inverted-output as discussed above (both of them having two inverters and one transmission gate delay).

With respect to claims 13 and 14, Figure 16A shows a first signal path between the first node and the non-inverted output node (DO) and a second signal path between the second node and the inverted output node (DO) each comprises the same number of circuit elements (two

inverters and one transmission gate as discussed in claim 12). Note, in claim 14, each of the first and second signal paths comprises two inverters.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakagami (JP 62-40816) in view of Weste et al. (Principles of CMOS VLSI Design: A Systems Perspective, 1993, Addison Wesley, 2nd Edition, page 91).

With respect to claim 1, Figure 14 of the Sakagami reference discloses a flip-flop which includes: a clock signal (ø); a data signal (DI/); a non-inverted output (DO); and inverted output (DO/); a first holding element (18_1-18_2) having first (N3) and second (N4) nodes; and a second holding element (18_3-18_4) having third (N6) and fourth (N5) nodes; wherein the first node is coupled to the fourth node via a first signal path (through 17_3) and the second node is coupled to the third node via a second signal path (through 17_4) exclusive of the first signal path. The flip-flop in Figure 14 does not disclose that the second signal path including a delay element in the form of a transmission gate. However, the Weste et al. disclose that a tristate inverter is easily constructed by cascading a transmission gate with an inverter (see Figure 2.37(a), lines 1-2 of paragraph 2.7). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to implement each of the tristate inverters in Figure 14 of the Sakagami reference by cascading a transmission gate with an inverter as taught in Figure 2.37(a) of Weste

at al. for the purpose of easy and simple in constructing the flip-flop circuit. Thus, this modification/combination meets all the limitations of claim 1 including the second signal path including a delay element in the form of a transmission gate (i.e., the transmission gate inside of the tristate inverter 17_4). Note that when clock ø = Hi (first level), then the first node having the logic value of the data signal DI/ while the second node having the logic level of inverted logic value of the data signal DI/; and when clock ø = Lo (second level), then the logic value DI/ at the first node is transferred and inverted to the fourth node, and the inverted logic value of DI/ at the second node is transferred and inverted to the third node; wherein the fourth node corresponding the non-inverted output and the third node corresponding to the inverted output.

Insofar as understood in claim 2, the above modification/combination shows the one of first and second feedback loops includes a negative-feed-back inverter circuit formed by two inverting logic elements connected back-to back (see 18_1-18_2 or 18_3-18_4).

With respect to claim 3, the above modification/combination shows the flip-flop further includes an inverter (17_2).

With respect to claim 4, the above modification/combination shows the first and second clock-controlled inverters (inverters 17_3 and 17_4).

Allowable Subject Matter

8. Claims 5, 8-11 and 15-20 are allowed. Claims 6 and 7 would be allowed if amended to overcome the informalities set forth above.

Claim 5 is allowed because the prior art of record fails to disclose or suggest a flip-flop which includes all the limitations of this claim. In particularly, the prior art of record fails to disclose or suggest that the flip-flop includes, in combination with other limitations, the a reset

signal and the second feedback loop comprising a NOR gate having a first input receiving the reset signal.

Claims 8-11 are allowed because they depend on claim 5.

Claim 6 and 7 would be allowed because they depend on claim 5.

Claim 15 are allowed because the prior art of record fails to disclose or suggest a resettable flip-flop which includes all the limitations of this claim. In particularly, the prior art of record fails to disclose or suggest that the resettable flip-flop includes, in combination with other limitations, the propagation delay of the non-inverted logic level from the first node the non-inverted output node equals to the propagation delay of the inverter level from the second node to the inverted-output node, and the first and second feedback loops each comprises a reset circuitry to place the inverted and non-inverted output nodes at known logic levels in response to a reset signal regardless of the state of the clock signal.

Claims 16-20 are allowed because they depend on claim 15.

Response to Arguments

9. Applicant's arguments filed on 2/22/05 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 11, 2005

LONG NGUYEN
PRIMARY EXAMINER